In the present application, those skilled in the art readily understand that the space below the insulating layer 3 represents one major surface of a semiconductor substrate. However, to provide additional clarity, applicant, at the suggestion of the Examiner, now labels the substrate 13 separately from the insulating layer 3. Indeed, the application filed clearly describes and teaches to those skilled in the art a conductive barrier 4 located over the insulating layer 3 in the recesses 2 and over the at least one major surface of the substrate (now labeled 13), and a conductive metal 8 in the recesses 2 only.

The thinness/thickness of the insulating layer 3 relative to the remainder of the substrate 13 is not essential to the claimed invention (amended claim 25), as is well understood by those skilled in the art.

Thus, applicant believes that any rejections/objections have been overcome without the introduction of new matter.

Accordingly, entry of this amendment, approval of the proposed drawing changes (filed 10/19/01), allowance of claims 25-32, and passage of this case to issue are respectfully requested.

Respectfully submitted,

Cyprian E. Uzoh, et al.

By: 3-28-02

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JPA/rmm

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

25. (Twice Amended) A semiconductor structure comprising a semiconductor substrate; recesses located in at least [on] one major surface of said semiconductor substrate; electrical insulating layer located [at least one major surface] over said at least one major surface and in said recesses; a conductive barrier located over said insulating layer in said recesses and over said at least one major surface; a plating seed layer located over said conductive barrier within said recesses only; and [an electroplated] a conductive metal in said recesses only.